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10/670,036

09/23/2003

Michael D. Flasz

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EXAMINER

ENGLUND, TERRY LEE

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------------|---|--|
| Office Action Summary | Application No. 10/670,036 | Applicant(s) FLASZA, MICHAEL D. | |
| | Examiner Terry L. Englund | Art Unit 2816 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on May 23, 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Pre-Appeal Brief Request

The Pre-Appeal Brief Request submitted on Nov 14, 2005 was reviewed and considered with the following results:

After reconsidering the applicant's comments, and attending a pre-appeal conference, it was determined that the finality of the previous Office Action would be withdrawn, and prosecution of the present application would be re-opened.

The prior art rejections described in the previous Office Action have been withdrawn. Those rejections include: 1) claims 1, 4, 8, 15-16, and 18 under 35 U.S.C. 102(e), and 2) claims 2-3, 5, 7, 9-12, 17, and 20 under 35 U.S.C. 103(e), all with respect to the reference of Saito et al. That reference does not clearly use the term "loop", or any variation of it. However, the examiner reserves the right to re-apply this reference, or any other reference, to the claimed limitations once the claimed limitations, and the invention, are more clearly understood.

Therefore, this Office Action is NON-FINAL.

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show how control 38 controls anything, and how resistor R can sense the loop current as described in the specification. For example, the node coupled in common to resistor R, control 38, capacitors C1-C3, diode D1, and control circuit 26 in the applicant's own Fig. 1 is actually shown coupled directly to ground. With such a ground connection, how is the loop current sensed, and where this loop current varied? Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing

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sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

After carefully reconsidering the disclosure, it is objected to because of the following informalities: Page 2, line 16 “place” should be --placed-- to improve word flow. Page 3 (line 20) and page 4 (line 19) both indicate the current within a loop is controlled. However, the applicants’ own figures and disclosure never clearly shows or discloses how this is actually accomplished. Therefore, it is suggested the wording, and/or figures, be changed to more accurately depict what is actually meant to be shown and disclosed. Page 4, line 11 is misleading since it appears to imply the cascaded charge pump circuits would not be connected to the control circuit if the regulator diode was not there. Using the applicants’ Fig. 1 for

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reference, diode D1 does have one terminal (i.e. its cathode) connected between cascaded charge pump circuits U1,U2 and control circuit 26. However, cascaded charge pump circuits U1,U2 and control circuit 26 would still be connected together, even if diode D1 was not present.

Therefore, it is suggested more accurate phrasing be used on page 4 (e.g. --a regulator diode is connected to the cascaded charge pump circuits and the control circuit--). The phrase "Further features and advantages of the invention will be readily apparent from the specification and from the drawings" on page 5, lines 7-8 are also misleading. If everything was clearly shown and disclosed, this examiner, and the various other examiners that were recently consulted about this application, would not be confused with respect to how the circuit operates, and how it is shown within the applicant's own Fig. 1. For example, it is still not known how control 38 controls the loop current, or how resistor R can sense current flowing within the loop since resistor R is clearly shown with one terminal coupled directly to ground, and the other terminal is coupled directly to the negative terminal of a remote power source. It is not understood how "instrument 12 varies the signal current in the loop between 4mA and 20mA DC" as cited on page 6, lines 2-3. For example, where in the loop is the current varied? It appears that current I1 of the applicants' Fig. 1 will be constant (e.g. see "3.5MA current source 40" on page 9, lines 8-9), and with resistor R coupled directly to ground, in what specific section of the applicants' circuit will the loop current actually vary? If the applicants' do not intend to limit the invention "to any particular type of instrument or measurement technique" as cited on page 6, lines 7-8, then what do the applicants' intend to mean by using "loop powered process control instrument power supply" in the title, and "loop powered process instrument" within the claims? For example, what do the applicants' mean by the use of "loop", "process", and "instrument" since none of

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these terms have been clearly defined within the disclosure, and they can all be interpreted in various ways? It is not understood how “output circuit 38 controls current on the loop 10 in accordance with the control signal on the line 36” as cited on page 6, lines 14-15. Again using the applicants’ Fig. 1 as a reference, control 38 is shown coupled between the positive terminal of power source 20 and ground, while also being coupled to the left terminal of resistor R, and receiving control signal 36. However, the circuit does not appear to show any output from control 38. After consulting with at least six other examiners, it was determined that possibly current source 40 may be some type of pass transistor, and control 38 might provide some type of control signal to the pass transistor’s control terminal, thus maintaining a constant current I1 (e.g. at 3.5mA) through current source 40. However, it is also possible that control 38 might somehow control internal clock 56 (e.g. see Fig. 2) within each charge pump circuit U1 and U2. Combined with the feedback signal, those ways described above would effectively vary the loop current. When considering the applicant’s own “4-20mA Current Loop Primer” reference submitted previously, it appears the loop current within that reference is controlled by a comparator with its positive and negative power supply terminals coupled in series within the loop. However, how does that type of structure relate to the present invention which apparently has the negative power supply terminal of control 38 connected directly to ground? Therefore, until the applicant clearly shows or describes how control 38 works, what it actually controls, and if the right terminal of resistor R is actually meant to be connected directly to ground, it will remain unknown to this examiner how the loop current within the applicants’ own Fig. 1 can be varied. Viewed in a slightly different manner, and using the applicant’s own Fig. 1 as a reference, it is understood that control circuit 26 is coupled between voltage V3 and ground,

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provides control signal 36, and has some type of connection to primary element 14. However, it is not understood what this control circuit can be, and how control signal 36 and the connection to 14 relate to one another. For example, a simple two resistor voltage divider coupled between voltage V3 and ground can provide a control signal from between the two resistors, wherein the connection to 14 could possibly be directly to either V3, control signal 36, or the common connection between the two resistors within the voltage divider. Also, it is believed control 38 could be a comparator coupled between 16 and ground for power, receiving the potential at node 18 as a reference signal, and receiving control signal 36 as the variable/comparison signal. However, as cited previously, it is not understood how control 38 actually controls the current through the loop, or even what (e.g. elements) it controls. For example, does control 38 have an output that controls current source 40, and/or somehow controls the switching within U1 and U2, or does control 38 control the voltage drop between node 16 and ground? As presently shown and described, it is understood control 38 is coupled in parallel with respect to power supply 20 and sense resistor R, wherein current source 40, charge pump circuits U1 and U2, and control circuit 26 are also coupled in parallel with 20 and R. Therefore, from the figure, and lack of specific details within the description, it is not understood where the loop current would actually be sensed or varied, and clarification is still requested with respect to how control circuit 26 “of any known design” (see page 7, lines 4-6) and control block 38 (see page 7, lines 12-14), can actually perform their function. Page 7, line 11 “senses” should be --sense-- to improve word flow. To be more consistent with labeling throughout the disclosure, it is suggested “instrument electronics” on lines 14 and 15 of page 10 be changed to “control circuit” (e.g. see lines 9 and 10 of the same page). Appropriate corrections and/or clarifications required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

After consulting with other examiners, claims 1-20 remain rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. How the loop current is actually sensed and controlled is considered by this examiner to be critical or essential to the practice and understanding of the invention. Therefore, these current related limitations included in the claim(s) are not enabled by the disclosure, and the circuit shown within Fig. 1. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Although control block 38, shown in Fig. 1, allegedly controls the loop current, and resistor R senses the loop current, the description and the circuit shown in Fig. 1 do not indicate how that is actually performed. As described above with respect to the disclosure and Fig. 1, control 38 does not appear to actually affect the loop's current since control 38 is simply shown connected between node 16 and ground, and in parallel with 20/R as well as with 40/U1/U2/26. Therefore, this type of configuration does not provide sufficient information to how the loop current will actually be controlled, or even how the loop current can actually be sensed by resistor R. For example, does control 38 control current source 40, one or both of the charge pump circuits U1 and U1, some combination of these elements, or possibly the voltage drop between node 16 and ground?

No claim is allowable.

Response to Arguments

The applicant's arguments filed Nov 14, 2005 have been fully considered but they are not persuasive. The applicant argues that: 1) what is conventional and known to those skilled in the art do not need to be described in detail; 2) an output circuit controls current on the loop in accordance with the control signal; 3) the objections to the specification and rejection of the claims are in clear error; 4) block 38 uses resistor R to sense loop current and controls the loop current; 5) Saito et al. is not directed to a process instrument, let alone a loop powered process instrument; and 6) while current is variable, it is not process variable and there is no two-wire process loop.

Related to most of the arguments described above (e.g. 1-4), the applicant is basically correct if the applicant's own figures are completely accurate with respect to what is conventional and known to those skilled in the art, and under those circumstances, the conventional and known do not need to be described in detail. However, this examiner strongly traverses the applicant's implication that the final rejections described in the previous Office Action are "clear errors." This examiner needs to know if the applicant's own figures are actually completely accurate, and no type of error is shown? For example, after consulting with numerous other examiners (i.e. at least six examiners scattered across four different classes), none of them could easily determine how the applicant's invention could work as shown within Fig. 1. Therefore, it is requested that the applicant clearly describe what comprises the loop, and how its current can be varied within the circuit shown in Fig. 1, wherein ground is apparently coupled directly to the negative power supply terminal of control 38. Also, a clear description of how resistor R can actually sense the loop current, and at least one good description or example

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on how control 38 will actually control that loop current, are requested with respect to the circuit presently shown within Fig. 1.

5) The applicant argues that the reference of Saito et al. is not directed to a process instrument, let alone a loop powered process instrument. However, where in the original disclosure is “process instrument” and “loop powered process instrument” clearly defined? It appears the applicant relies more on labels than actually circuitry. For example, any type of circuitry that senses, detects, monitors, generates, or provides something is one type of an instrument (e.g. circuit) that processes something (e.g. current or voltage). If there is any type of feedback within that circuit/instrument, that feedback provides a loop that effectively powers the circuit/instrument. For example, without the feedback, the circuit/instrument would not function the same way, or function efficiently. Therefore, the circuit requires the feedback (loop) to power (or operate) the circuit/ instrument. However, perhaps the applicant intends to mean the process instrument is actually powered by the loop, wherein the loop by itself actually provides the power (e.g. voltages) required for the circuit/instrument to operate, but this is never clearly disclosed. Using the applicant’s own “4-20mA Current Loop Primer” as a reference, a comparator is shown with its positive and negative power supply terminals coupled in series within a clear loop structure. However, since the applicant’s own Fig. 1 circuit is clearly shown with the negative power supply terminal apparently coupled directly to ground, how would the applicant’s circuit work, and how does such a structure actually relate to the circuitry shown in the Primer, which has no apparent connection to a ground?

6) The applicant also argues that while current is variable, it is not process variable and there is no two-wire process loop. Again it comes back to what does the applicant mean by the

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label “process”, which has not been clearly defined within the original disclosure? Also, if a circuit has a feedback line, why wouldn’t that type of circuit be considered a “two-wire process loop.” The circuit has at least two wires (e.g. one providing a current or signal to another part of the circuit, and one providing a feedback related control signal to some part of the circuitry that will help control at least part of the overall circuitry, and thus will have one type of loop control. Therefore, that is one type of process control using the broadest reasonable interpretation of those terms.

From the consultations this examiner has had with the various other examiners, and until the applicant can both verify that the circuit shown in Fig. 1 is entirely accurate, and can clearly describe or explain how the Fig. 1 circuit can actually sense and control the loop current, it is strongly believed the rejections described within the present application are proper with respect to what is actually shown and disclosed.

No prior art rejections have been made in the present Office Action. However, once a better understanding of the claimed invention’s limitations are known, with a respect to the circuit presently shown within the applicant’s own Fig. 1, it is possible prior art rejections can be made in the future.

This Office Action is NON-FINAL.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Tim Callahan, can be reached on (571) 272-1740.

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The new central official fax number is (571) 273-8300.


Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

28 February 2006



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